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# DATA SHEET



# UDA1335H
# Universal Serial Bus (USB) Audio Playback Recording Peripheral (APRP)

Preliminary specification
File under Integrated Circuits, IC01

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Philips
Semiconductors


PHILIPS

# Universal Serial Bus (USB) Audio Playback Recording Peripheral (APRP)

# UDA1335H

## FEATURES

### General

- USB stereo audio record and playback system with 20 bits analog-to-digital conversion (with 5 to 55 kHz sample frequency range) and adaptive 20 bits digital-to-analog conversion (with 5 to 55 kHz sample frequency range) with integrated filtering
- USB-compliant audio/HID device
- Supports 12 Mbits/s 'full speed' serial data transmission
- Fully automatic 'Plug-and-Play' operation
- Supports multiple audio data formats (8, 16 and 24 bits)
- 5.0 and 3.3 V power supply
- Low power consumption
- Efficient power management
- On-chip master clock oscillators, only an external crystal is required
- High linearity
- Wide dynamic range
- Superior signal-to-noise ratio
- Low total harmonic distortion
- Supports headphone and line output
- Partly programmable USB descriptors and configuration via the I$^2$C-bus.

### Sound processing (for digital-to analog conversion)

- Separate digital volume control for left and right channel
- Soft mute
- Digital bass and treble tone control
- External Digital Sound Processor (DSP) option possible via standard I$^2$S-bus or Japanese digital I/O format
- Selectable clipping prevention
- Selectable Dynamic Bass Boost (DBB)
- On-chip digital de-emphasis.

### Document references

- *"USB Specification"*
- *"USB Device Class Definition for Audio Devices"*
- *"Device Class Definition for Human Interface Devices (HID)"*
- *"USB HID Usage Table"*
- *"USB Common Class Specification"*.

## GENERAL DESCRIPTION

The UDA1335H is a stereo CMOS codec incorporating bitstream converters designed for implementation in USB-compliant audio peripherals and multimedia audio applications. The UDA1335H is an adaptive asynchronous sink USB audio device with a continuous sampling frequency range from 5 to 55 kHz. It contains a USB interface, an embedded microcontroller, an Analog-to-Digital Interface (ADIF) and an Asynchronous Digital-to-Analog Converter (ADAC).

The USB interface is the interface between the USB, the ADIF, the ADAC and the microcontroller. The USB interface consists of an analog front-end and a USB processor. The analog front-end transforms the differential USB data into a digital data stream. The USB processor buffers the incoming and outgoing data from the analog front-end and handles all low-level USB protocols.
The USB processor selects the relevant data from the universal serial bus, performs an extensive error detection and separates control information (input and output) and audio information (input and output). The control information is made accessible to the microcontroller. The audio information received from the PC becomes available at the digital I/O output or is fed directly to the ADAC. The audio information to be transmitted to the PC is delivered by the ADIF or by the digital I$^2$S-bus interface.

The microcontroller handles the high-level USB protocols, translates the incoming control requests and manages the user interface via general purpose pins and an I$^2$C-bus.

The firmware for the microcontroller must be located in an external (E)PROM.

The ADAC enables the wide and continuous range of input sampling frequencies. By means of a Sample Frequency Generator (SFG), the ADAC is able to reconstruct the average sample frequency from the incoming audio samples. The ADAC also performs the sound processing. The ADAC consists of a FIFO, a unique audio feature processing DSP, the SFG, digital upsampling filters, a variable hold register, a Noise Shaper (NS) and a Filter Stream DAC (FSDAC) with integrated filter and line output drivers. The audio information is applied to the ADAC via the USB processor or via the digital I/O input.

The ADIF consists of an Programmable Gain Amplifier (PGA), an Analog-to-Digital Converter (ADC) and a Decimator Filter (DF). An Analog Phase Lock Loop (APLL) or oscillator is used for clocking the ADIF. The clock frequency for the ADIF can be controlled via the microcontroller. Several clock frequencies are possible for sampling the analog input signal at different sampling rates.

Via the digital I/O-bus, an external DSP can be used for adding extra sound processing features for the audio received from the PC.

The UDA1335H supports the digital I/O and the $I^2S$-bus interface, with standard $I^2S$-bus data input format and the LSB justified serial data input format with word lengths of 16, 18 and 20 bits.

The wide dynamic range of the bitstream conversion technique used in the UDA1335H guarantees a high audio sound quality.

## APPLICATIONS

- USB monitors
- USB speakers
- USB headsets
- USB telephone/answering machines
- USB links in consumer audio devices.

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| UDA1335H | QFP64 | plastic quad flat package; 64 leads (lead length 1.95 mm); body $14 \times 20 \times 2.8$ mm | SOT319-2 |

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Supplies** | | | | | | |
| $V_{DDE}$ | supply voltage periphery | | 4.75 | 5.0 | 5.25 | V |
| $V_{DDI}$ | supply voltage core | | 3.0 | 3.3 | 3.6 | V |
| $I_{DD(tot)}$ | total supply current | | – | 60 | tbf | mA |
| $I_{DD(tot)(ps)}$ | total supply current in power-saving mode | note 1 | – | 360 | – | μA |
| **Dynamic performance DAC** | | | | | | |
| (THD + N)/S | total harmonic distortion plus noise-to-signal ratio | $f_s$ = 44.1 kHz; $R_L$ = 5 kΩ | | | | |
| | | $f_i$ = 1 kHz (0 dB) | – | –90 | –80 | dB |
| | | | – | 0.0032 | 0.01 | % |
| | | $f_i$ = 1 kHz (–60 dB) | – | –30 | –20 | dB |
| | | | – | 3.2 | 10 | % |
| S/N | signal-to-noise ratio at bipolar zero | A-weighted at code 0000H | 90 | 95 | – | dBA |
| $V_{o(FS)(rms)}$ | full-scale output voltage (RMS value) | $V_{DD}$ = 3.3 V | – | 0.66 | – | V |
| **Dynamic performance PGA and ADC** | | | | | | |
| (THD + N)/S | total harmonic distortion plus noise-to-signal ratio | $f_s$ = 44.1 kHz; PGA gain = 0 dB | | | | |
| | | $f_i$ = 1 kHz; (0 dB); $V_i$ = 1.0 V (RMS) | – | –85 | –80 | dB |
| | | | – | 0.0056 | 0.01 | % |
| | | $f_i$ = 1 kHz (–60 dB) | – | –30 | –20 | dB |
| | | | – | 3.2 | 10.0 | % |
| S/N | signal-to-noise ratio | $V_i$ = 0.0 V | 90 | 95 | – | dBA |
| **General characteristics** | | | | | | |
| $f_{i(s)}$ | audio input sample frequency | | 5 | – | 55 | kHz |
| $T_{amb}$ | operating ambient temperature | | 0 | 25 | 70 | °C |

**Note**

1. Exclusive the $I_{DDE}$ current which depends on the components connected to the I/O pins.

## BLOCK DIAGRAM

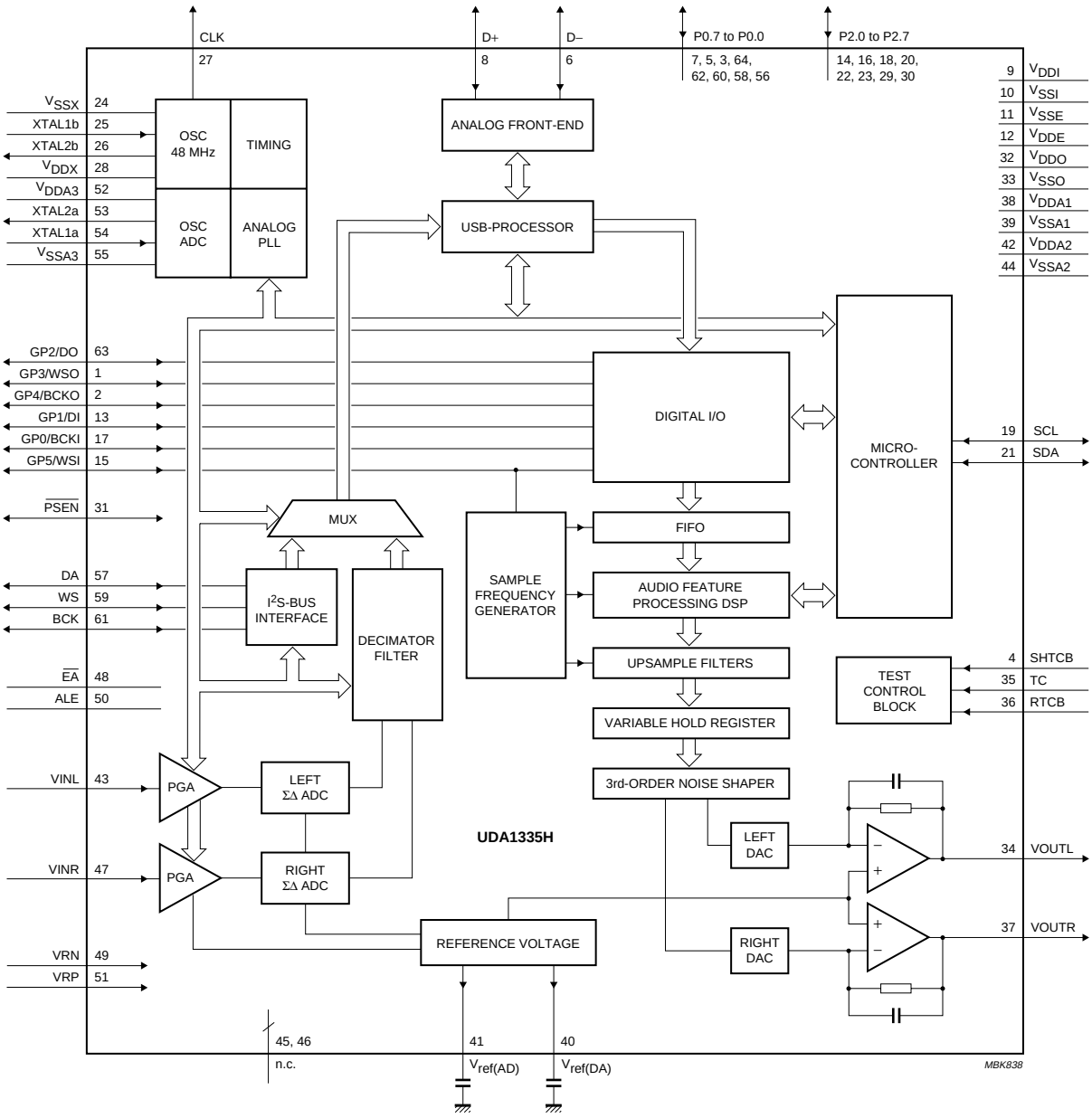



Fig.1 Block diagram.

**PINNING**

| SYMBOL | PIN QFP64 | I/O | DESCRIPTION |
|---|---|---|---|
| GP3/WSO | 1 | I/O | general purpose pin 3 or word select output |
| GP4/BCKO | 2 | I/O | general purpose pin 4 or bit clock output |
| P0.5 | 3 | I/O | port 0.5 of the microcontroller |
| SHTCB | 4 | I | shift clock of the test control block (active HIGH) |
| P0.6 | 5 | I/O | port 0.6 of the microcontroller |
| D– | 6 | I/O | negative data line of the differential data bus, conforms to the USB standard |
| P0.7 | 7 | I/O | port 0.7 of the microcontroller |
| D+ | 8 | I/O | positive data line of the differential data bus, conforms to the USB standard |
| $V_{DDI}$ | 9 | – | digital supply voltage for core |
| $V_{SSI}$ | 10 | – | digital ground for core |
| $V_{SSE}$ | 11 | – | digital ground for I/O pads |
| $V_{DDE}$ | 12 | – | digital supply voltage for I/O pads |
| GP1/DI | 13 | I/O | general purpose pin 1 or data input |
| P2.0 | 14 | I/O | port 2.0 of the microcontroller |
| GP5/WSI | 15 | I/O | general purpose pin 5 or word select input |
| P2.1 | 16 | I/O | port 2.1 of the microcontroller |
| GP0/BCKI | 17 | I/O | general purpose pin 0 or bit clock input |
| P2.2 | 18 | I/O | port 2.2 of the microcontroller |
| SCL | 19 | I/O | serial clock line $I^2C$-bus |
| P2.3 | 20 | I/O | port 2.3 of the microcontroller |
| SDA | 21 | I/O | serial data line $I^2C$-bus |
| P2.4 | 22 | I/O | port 2.4 of the microcontroller |
| P2.5 | 23 | I/O | port 2.5 of the microcontroller |
| $V_{SSX}$ | 24 | – | crystal oscillator ground (48 MHz) |
| XTAL1b | 25 | I | crystal input (analog; 48 MHz) |
| XTAL2b | 26 | O | crystal output (analog; 48 MHz) |
| CLK | 27 | O | 48 MHz clock output signal |
| $V_{DDX}$ | 28 | – | supply crystal oscillator (48 MHz) |
| P2.6 | 29 | I/O | port 2.6 of the microcontroller |
| P2.7 | 30 | I/O | port 2.7 of the microcontroller |
| $\overline{PSEN}$ | 31 | I/O | program store enable (active LOW) |
| $V_{DDO}$ | 32 | – | supply voltage for operational amplifier |
| $V_{SSO}$ | 33 | – | operational amplifier ground |
| VOUTL | 34 | O | voltage output left channel |
| TC | 35 | I | test control input (active HIGH) |
| RTCB | 36 | I | asynchronous reset input of the test control block (active HIGH) |
| VOUTR | 37 | O | voltage output right channel |
| $V_{DDA1}$ | 38 | – | analog supply voltage 1 |
| $V_{SSA1}$ | 39 | – | analog ground 1 |

| SYMBOL | PIN QFP64 | I/O | DESCRIPTION |
|---|---|---|---|
| $V_{ref(DA)}$ | 40 | O | reference voltage output DAC |
| $V_{ref(AD)}$ | 41 | O | reference voltage output ADC |
| $V_{DDA2}$ | 42 | – | analog supply voltage 2 |
| VINL | 43 | I | input signal left channel PGA |
| $V_{SSA2}$ | 44 | – | analog ground 2 |
| n.c. | 45 | – | not connected |
| n.c. | 46 | – | not connected |
| VINR | 47 | I | input signal right channel PGA |
| $\overline{EA}$ | 48 | – | external access (active LOW) |
| VRN | 49 | I | negative reference input voltage ADC |
| ALE | 50 | – | address latch enable (active HIGH) |
| VRP | 51 | I | positive reference input voltage ADC |
| $V_{DDA3}$ | 52 | – | supply voltage for crystal oscillator and analog PLL |
| XTAL2a | 53 | O | crystal output (analog; ADC) |
| XTAL1a | 54 | I | crystal input (analog; ADC) |
| $V_{SSA3}$ | 55 | – | crystal oscillator and analog PLL ground |
| P0.0 | 56 | I/O | port 0.0 of the microcontroller |
| DA | 57 | I | data Input (digital) |
| P0.1 | 58 | I/O | port 0.1 of the microcontroller |
| WS | 59 | I | word select input (digital) |
| P0.2 | 60 | I/O | port 0.2 of the microcontroller |
| BCK | 61 | I | bit clock input (digital) |
| P0.3 | 62 | I/O | port 0.3 of the microcontroller |
| GP2/DO | 63 | I/O | general purpose pin 2 or data output |
| P0.4 | 64 | I/O | port 0.4 of the microcontroller |

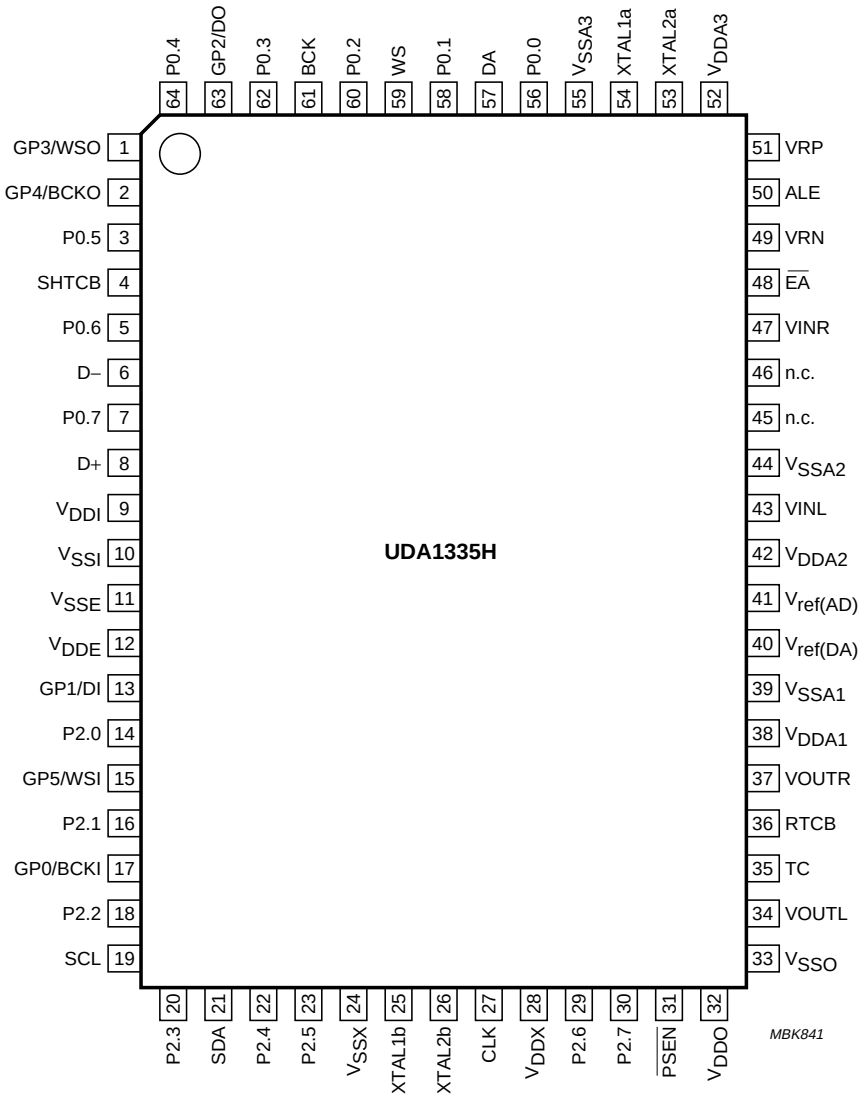



Fig.2 Pin configuration.

## FUNCTIONAL DESCRIPTION

### The Universal Serial Bus (USB)

Data and power is transferred via the USB over a 4-wire cable. The signalling occurs over two wires and point-to-point segments. The signals on each segment are differentially driven into a cable of 90 Ω intrinsic impedance. The differential receiver features input sensitivity of at least 200 mV and sufficient common mode rejection.

### The analog front-end

The analog front-end is an on-chip generic USB transceiver. It is designed to allow voltage levels up to $V_{DD}$ from standard or programmable logic to interface with the physical layer of the USB. It is capable of receiving and transmitting serial data at full speed (12 Mbits/s).

### The USB processor

The USB processor forms the interface between the analog front-end, the ADIF, the ADAC and the microcontroller. The USB processor consists of:

- The Philips Serial Interface Engine (PSIE)
- The Memory Management Unit (MMU)
- The Audio Sample Redistribution (ASR) module.

### The Philips Serial Interface Engine and Memory Management Unit (PSIE/MMU)

The PSIE/MMU translates the electrical USB signals into bytes and signals. Depending upon the USB device address and the USB endpoint address, the USB data is directed to the correct endpoint buffer on the PSIE/MMU interface. The data transfer could be of bulk, isochronous, control or interrupt type. The USB device address is configured during the enumeration process.

The UDA1335H has four endpoints. These are:

- Control endpoint 0
- Status interrupt endpoint
- Isochronous data sink endpoint
- Isochronous data source endpoint.

The amount of bytes/packet on the control endpoint is limited by the PSIE/MMU hardware to 8 bytes/packet.

The PSIE is the digital front-end of the USB processor. This module recovers the 12 MHz USB clock, detects the USB sync word and handles all low-level USB protocols and error checking.

The MMU is the digital back-end of the USB processor. It handles the temporary data storage of all USB packets that are received or sent over the bus. Three types of packets are defined on the USB. These are:

- Token packets
- Data packets
- Handshake packets.

The token packet contains information about the destination of the data packet. The audio data is transferred via an isochronous data sink endpoint or source endpoint and, consequently, no handshaking mechanism is used. The MMU also generates a 1 kHz clock that is locked to the USB Start Of Frame (SOF) token.

### The Audio Sample Redistribution (ASR)

The ASR reads the audio samples from the MMU and distributes these samples equidistant over a 1 ms frame period. The distributed audio samples are translated by the digital I/O module to standard $I^2S$-bus format or Japanese digital I/O format. The ASR generates the bit clock and the word select signal of the digital I/O.
The digital I/O formats the received audio samples to one of the four specified serial digital audio formats ($I^2S$-bus, 16, 18 or 20 bits LSB-justified).

### The microcontroller

The microcontroller receives the control information selected from the USB by the USB processor. It handles the high-level USB protocols and the user interfaces.

The major task of the software process, that is mapped upon the microcontroller, is to control the different modules of the UDA1335H in such a way that it behaves as a USB device.

Therefore the microcontroller:

- Interprets the USB requests and maps them upon the UDA1335H application
- Controls the internal operation of the UDA1335H, the digital I/O pins and the GP I/O pins
- Communicates with the external world (external controller, EEPROM) using the $I^2C$-bus facility and the GP I/O pins.

The microcontroller does not handle the audio stream. The UDA1335H will be delivered with USB compliant firmware. The firmware must be located in an external (E)PROM.

### The Analog-to-Digital Interface (ADIF)

The ADIF is used for sampling an analog input signal from a microphone or line input and sending the audio samples to the USB interface. The ADIF consists of a stereo Programmable Gain Amplifier (PGA), a stereo Analog-to-Digital Converter (ADC) and Decimation Filters (DFs). The sample frequency of the ADC is determined by the ADC clock (see Section “The timing of the analog-to-digital interface”). The user can also select a digital serial input instead of an analog input. In this event the sample frequency is determined by the continuous WS clock with a range between 5 to 55 kHz. Digital serial input is possible with four formats ($I^2S$-bus, 16, 18 or 20 bits LSB-justified).

### The Programmable Gain Amplifier circuit (PGA)

This circuit can be used for a microphone or line input. The input audio signals can be amplified by 7 different gains. The preferred gain is selected during start-up of the device (configuration map).

The gain settings are given in Table 1.

**Table 1** The selectable gains of the PGA

| SETTING | GAIN | UNIT |
|---|---|---|
| 000 | –3 | dB |
| 001 | 0 | dB |
| 010 | 3 | dB |
| 011 | 9 | dB |
| 100 | 15 | dB |
| 101 | 21 | dB |
| 11X | 27 | dB |

### The Analog-to-Digital Converter (ADC)

The stereo ADC of the UDA1335H consists of two 3rd-order Sigma-Delta modulators. They have a modified Ritchie-coder architecture in a differential switched capacitor implementation. The oversampling ratio is 128. Both ADCs can be switched off in power saving mode (left and right separate). The ADC clock is generated by the analog PLL or the ADC oscillator.

### The Decimation Filter (DF)

The decimator filter converts the audio data from $128f_s$ down to $1f_s$ with a word width of 8, 16 or 24 bits. This data will be transmitted over the USB as mono or stereo in 1, 2 or 3 bytes/sample. The decimator filters are clocked by the ADC clock.

### The timing of the analog-to-digital interface

The clock source of the ADIF is the analog PLL or the ADC oscillator. The preferred clock source can be selected during start-up of the device (configuration map). The ADC clock used for the ADC and decimation filters is obtained by dividing the clock signal coming from the analog PLL or from the ADC oscillator by a factor Q.

Using the analog PLL the user can select 3 clock frequencies via the microcontroller.

By connecting the appropriate crystal the user can choose any clock signal between 8.192 and 14.08 MHz via the ADC oscillator.

**Table 2** The analog PLL clock output frequencies

| FCODE | APLL CLOCK FREQUENCY (MHz) |
|---|---|
| 00 | 11.2896 |
| 01 | 8.1920 |
| 10 | 12.2880 |
| 11 | 11.2896 |

The dividing factor Q can be selected via the microcontroller. With this dividing factor Q the user can select a range of ADC clock signals allowing several different sample frequencies (see Table 3).

**Table 3** ADC clock frequencies and sample frequencies based upon using the APLL as a clock source (analog input topology 1), see note 1.

| APLL CLOCK FREQUENCY (MHz) | DIVIDE FACTOR Q | ADC CLOCK FREQUENCY (MHz) | SAMPLE FREQUENCY (kHz) |
|---|---|---|---|
| 8.1920 | 1 | 4.096 | 32 |
| | 2 | 2.048 | 16 |
| | 4 | 1.024 | 8 |
| | 8 | 0.512 (not supported) | 4 (not supported) |
| 11.2896 | 1 | 5.6448 | 44.1 |
| | 2 | 2.8224 | 22.05 |
| | 4 | 1.4112 | 11.025 |
| | 8 | 0.7056 | 5.5125 |
| 12.2880 | 1 | 6.144 | 48 |
| | 2 | 3.072 | 24 |
| | 4 | 1.536 | 12 |
| | 8 | 0.768 | 6 |

**Note**

1. By using the APLL as a clock source 12 sample frequencies will be reported to the USB host.

**Table 4** ADC clock frequencies and sample frequencies based upon using the OSCAD as a clock source (analog input topology 4), see note 1

| OSCAD CLOCK FREQUENCY (MHz) | DIVIDE FACTOR Q | ADC CLOCK FREQUENCY (MHz) | SAMPLE FREQUENCY (kHz) |
|---|---|---|---|
| $f_{osc}$[2] | Q[3] | $f_{osc}/(2Q)$ | $f_{osc}/(256Q)$[4] |

**Notes**

1. By using the OSCAD as a clock source, the sample frequency and the Q dividing factor must be filled in the configuration map. Only this one sample frequency will be reported to the USB host.
2. The oscillator frequency (and therefore the crystal) of OSCAD must be between 8.192 and 14.08 MHz.
3. The Q factor can be 1, 2, 4 or 8.
4. Sample frequencies below 5 kHz and above 55 kHz are not supported.

### The Asynchronous Digital-to-Analog Converter (ADAC)

The ADAC receives USB audio information from the USB processor or from the digital I/O-bus. The ADAC is able to reconstruct the sample clock from the rate at which the audio samples arrive and handles the audio sound processing. After the processing, the audio signal is upsampled, noise-shaped and converted to analog output voltages capable of driving a line output. The ADAC consists of:

- A Sample Frequency Generator (SFG)
- FIFO registers
- An audio feature processing DSP
- Two digital upsampling filters and a variable hold register
- A digital Noise Shaper (NS)
- A Filter Stream DAC (FSDAC) with integrated filter and line output drivers.

### The Sample Frequency Generator (SFG)

The SFG controls the timing signals for the asynchronous digital-to-analog conversion. By means of a digital PLL, the SFG automatically recovers the applied sampling frequency and generates the accurate timing signals for the audio feature processing DSP and the upsampling filters.

### First-In First-Out (FIFO) registers

The FIFO registers are used to store the audio samples temporarily coming from the USB processor or from the digital I/O input. The use of a FIFO (in conjunction with the SFG) is necessary to remove all jitter present on the incoming audio signal.

### The audio feature processing DSP

A DSP processes the sound features. The control and mapping of the sound features is explained in Section “Controlling the USB APRP”. Depending on the sampling rate ($f_s$) the DSP knows four frequency domains in which the treble and bass are regulated. The domain is chosen automatically.

**Table 5** Frequency domains for audio processing by the DSP

| DOMAIN | SAMPLE FREQUENCY (kHz) |
|---|---|
| 1 | 5 to 12 |
| 2 | 12 to 25 |
| 3 | 25 to 40 |
| 4 | 40 to 55 |

### The upsampling filters and variable hold function

After the audio feature processing DSP two upsampling filters and a variable hold function increase the oversampling rate to $128f_s$.

### The noise shaper

A 3rd-order noise shaper converts the oversampled data to a noise-shaped bitstream for the FSDAC. The in-band quantization noise is shifted to frequencies well above the audio band.

### The Filter Stream DAC (FSDAC)

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. A post filter is not needed because of the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

### USB Audio Playback Recording Peripheral (APRP) descriptors

In a typical USB environment the PC has to know which kind of devices are connected. For this purpose each device contains a number of USB descriptors. These descriptors describe, from different points of view (USB configuration, USB interface and USB endpoint), the capabilities of a device. Each of them can be requested by the host. The collection of descriptors is denoted as a descriptor map. This descriptor map will be reported to the USB host during enumeration and on request.

The USB descriptors and their most important fields, in relationship to the characteristics of the UDA1335H are explained briefly below.

### AUDIO FUNCTION TOPOLOGIES

Four audio function Input topologies and two audio function output topologies are supported by the UDA1335H. Each configuration map can select only one Input and one output topology. The descriptors and the supported requests depend on the selected topologies in the active configuration map. Figures 3 and 4 illustrate the different audio Input and output topologies.

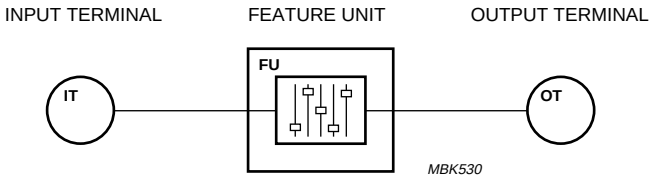
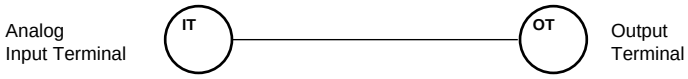
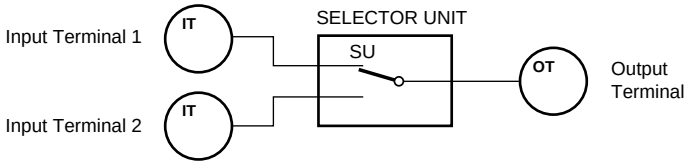


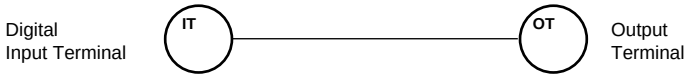

Fig.3 One audio output function topology (with or without bass boost) is supported.




a. Analog topology 1 (using APLL clock source).




b. Analog topology 2.




c. Digital topology 3.


d. Analog topology 4 (using OSCAD clock source).

Fig.4 Four input function topologies are supported.

### General descriptors

The UDA1335H supports one configuration containing a control interface, two audio interfaces and a HID interface. The descriptor map that describes this configuration is partly fixed and partly programmable.

The programmable part can be retrieved from one of four configuration maps located in the firmware or from an $I^2C$-bus EEPROM. At start-up time one of four internal configuration maps can be selected depending on the logical combination of GP3 and GP4. It is possible to overwrite this configuration map with a configuration map loaded from an $I^2C$-bus EEPROM.

### Audio device class specific descriptors

The audio device class is partly specified with standard descriptors and partly with specific audio device class descriptors. The standard descriptors specify the number and the type of the interface or endpoint. The UDA1335H supports 7 different audio modes:

- 8-bit PCM mono or stereo audio data
- 16-bit PCM mono or stereo audio data
- 24-bit PCM mono or stereo audio data
- Zero bandwidth mode.

Each mode is defined as an alternate setting of the audio interface, selectable with the standard audio streaming interface descriptor **bAlternateSetting** field.

The seven alternate settings are described in more detail by the specific audio device class descriptors.

The UDA1335H supports the input terminal, output terminal and the feature unit descriptors.

The input and output terminals are not controllable via the USB. The feature unit provides the basic manipulation of the incoming logical channels.

The supported sound features are:

- Volume control
- Mute control
- Treble control
- Bass control
- Bass Boost control.

The maximum number of audio data samples within a USB packet arriving on the isochronous sink endpoint is restricted by the buffer capacity of this isochronous endpoint. The maximum buffer capacity is 336 bytes/ms.

The input terminals can be defined by means of **wTerminalType.**

### The standard audio streaming interface descriptor for the isochronous data sink endpoint

In this section the descriptors are given for interface 1 which is used for receiving isochronous audio data from the host.

Although in this specific UDA1335H application no endpoint control properties can be used on the isochronous adaptive sink endpoint, the descriptors are still necessary to inform the host about the definition of this endpoint: isochronous, adaptive, sink, continuous sampling frequency (at input side of this endpoint) with a lower boundary of 5 kHz and an upper boundary of 55 kHz.

The audio class specific descriptors can be requested with the ‘Get Descriptor: configuration request’, which returns all the descriptors, except the device descriptor.

For each alternate setting with audio, a maximum bandwidth is claimed as indicated in the standard isochronous audio data endpoint descriptor **wMaxPacketSize** field. To allow a small overshoot in the number of audio samples per packet, the top sample frequency of 55 kHz is taken in the calculation of the bandwidth for each alternate setting. For each alternate setting, with its own isochronous audio data endpoint descriptor, **wMaxPacketSize** field is then defined as described in Table 6.

**Table 6** Audio bandwidth at each audio mode

| ALTERNATE SETTING | AUDIO MODE | wMaxPacketSize (HEX) |
|---|---|---|
| 1 | 8-bit PCM, mono | 3800 |
| 2 | 8-bit PCM, stereo | 7000 |
| 3 | 16-bit PCM, mono | 7000 |
| 4 | 16-bit PCM, stereo | E000 |
| 5 | 24-bit PCM, mono | A800 |
| 6 | 24-bit PCM, stereo | 5001 |

### The standard audio streaming interface descriptor for the isochronous data source endpoint

Interface 2 is used for sending isochronous audio data to the host. It has the same alternate settings as interface 1.

HUMAN INTERFACE DEVICE SPECIFIC DESCRIPTORS

The inputs defined on the UDA1335H are transmitted via the USB to the host according to the HID class. The host responds with the appropriate settings via the audio device class for the audio related parts or via the HID class for the HID related inputs and outputs of the UDA1335H.

A HID descriptor is necessary to inform the host about the conception of the user interface. The host communicates via the HID device driver using either the control pipe or the interrupt pipe. The UDA1335H is using USB endpoint 0 (control pipe) to respond to the HID specific 'Get/Set Report request' to receive or transmit data from or to the UDA1335H. The UDA1335H uses the status interrupt endpoint as interrupt pipe for polling asynchronous data.

The UDA1335H is a high-speed device. The maximum transaction size is 64 bytes per USB frame and the polling rate is defined at a maximum of every 1 ms.

The host requests the configuration descriptor which includes the standard interface descriptor, the HID endpoint descriptor and the HID descriptor. The HID device driver of the host then requests the report descriptor.

Report descriptors are composed of pieces of information about the device. Each piece of information is called an item. All items have a 1-byte prefix that contains the item tag, type and size. In the UDA1335H only the short item basic type is used.

The hosts HID device driver will parse the report descriptor and the defined items. By examining all of these items, the HID class driver is able to determine the size and composition of data reports from the device.

The main items of the UDA1335H are input reports. Input reports are sent via the interrupt pipe (UDA1335H USB endpoint 3). Input reports can be requested by the host via the control endpoint (USB endpoint 0).

The UDA1335H supports a maximum of two push-buttons (six with $I^2C$-bus expanders), which represent a certain feature of the UDA1335H.

If pressed by the user the pushbutton will go to its 'ON' state, if not pressed the push-button will go back to its 'OFF' state.

For more information about the input functions of the UDA1335H see the application documentation of the device.

**Controlling the USB APRP**

The sound features as defined in the *"USB Device Class Definition for Audio Devices"* are mapped on the UDA1335H specific feature registers by the microcontroller. These specific sound features are:

- Volume control (separate for left and right stereo channels, no master channel)
- Mute control (only master channel)
- Treble control (only master channel)
- Bass control (only master channel)
- Dynamic bass boost control (only master channel).

These specific features can be activated via the host (audio device class requests) or via the GP I/O pins (HID plus audio device class requests). The user is able to download the necessary configuration data for different applications (definition of the function of the GP pins, with or without digital I/O functionality etc.) via the configuration map. The mapping and control of the standard USB audio features and UDA1335H specific features is described below.

**Volume control**

Volume control is possible via the host or via predefined GP I/O pins. The setting of 0 dB is always referenced to the maximum available volume setting. Table 7 gives the mapping of **wVolume** value (as defined in the *"USB Device Class Definition for Audio Devices"*) upon the actual volume setting of the USB APRP. When using the UDA1335H, the range is 0 dB down to −60 dB (in steps of 1 dB) and $-\infty$ dB. Independant control of 'left'/'right' volume is possible.

It should be noted that $\mathbf{wVolume}_{LSB}$ B7 to B0 are not used. Values above 0 dB are returned as 0 dB.
The volume value at start-up of the device is defined in the selected configuration map.

Balance control is possible via the separate volume control option of both channels. Therefore the characteristics of the balance control are equal to the volume control characteristics.

**Table 7** Volume control characteristics

| wVOLUME (MSB) | | | | | | | | VOLUME USB SIDE (dB) | VOLUME USB APRP (dB) |
|---|---|---|---|---|---|---|---|---|---|
| **B15** | **B14** | **B13** | **B12** | **B11** | **B10** | **B9** | **B8** | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | –1 | –1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | –2 | –2 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | –3 | –3 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | –4 | –4 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | –5 | –5 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | –6 | –6 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | –7 | –7 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | –8 | –8 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | –9 | –9 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | –10 | –10 |
| ... | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | –59 | –59 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | –60 | –60 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | –61 | –∞ |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | –62 | –∞ |
| ... | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | –∞ | –∞ |

### Mute control

Mute is one of the sound features as defined in the *"USB Device Class Definition for Audio Devices"*. The mute control request data **bMute** controls the position of the mute switch. The position can be either on or off. When **bMute** is true the feature unit is muted. When **bMute** is false the feature unit is not muted.

When the mute is active for the master channel, the value of the sample is decreased smoothly to zero following a raised cosine curve. There are 32 coefficients used to step down the value of the data, each one being used 32 times before stepping to the next. This amounts to a mute transition of 23 ms at $f_s$ = 44.1 kHz. When the mute is released, the samples are returned to the full level again following a raised cosine curve with the same coefficients being used in reversed order.

The mute, on the master channel is synchronized to the sample clock, so that operation always takes place on complete samples.

A mute can be given via the host or by pressing a predefined GP pin.

### Treble control

The treble control is available for the master channel of the UDA1335H. The treble range is from 0 to 6 dB in steps of 2 dB. It should be noted that the negative treble values as defined in the *"USB Device Class Definition for Audio Devices"* are not supported by the UDA1335H; values below 0 dB are returned as 0 dB. The corner frequency is 1500 Hz. Table 8 gives the mapping of the **bTreble** value upon the actual treble setting of the USB APRP.

**Table 8** Treble control characteristics

| bTREBLE | | | | | | | | TREBLE USB HOST (dB) | TREBLE USB APRP (dB) |
|---|---|---|---|---|---|---|---|---|---|
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.00 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0.25 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0.50 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0.75 | |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1.00 | |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1.25 | 2 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1.50 | |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1.75 | |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 2.00 | |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 2.25 | |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 2.50 | |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 2.75 | |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 3.00 | |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 3.25 | 4 |
| | | | | | | | | ... | |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 5.25 | 6 |
| | | | | | | | | ... | |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 7.25 | 6 |
| | | | | | | | | ... | |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 9.25 | 6 |
| | | | | | | | | ... | |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 31.75 | 6 |

### Bass control

The bass control is available for the master channel of the UDA1335H. The bass range is from 0 to approximately 24 dB in steps of 2 dB. It should be noted that the negative bass values as defined in the *"USB Device Class Definition for Audio Devices"* are not supported by the UDA1335H; values below 0 dB are returned as 0 dB. The corner frequency is 75 Hz. Table 9 gives the mapping of the **bBass** value upon the actual bass setting of the USB APRP.

**Table 9** Bass control characteristics

| bBASS | | | | | | | | BASS USB HOST (dB) | BASS USB APRP (dB) |
|---|---|---|---|---|---|---|---|---|---|
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.00 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0.25 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0.50 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0.75 | |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1.00 | |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1.25 | 1.7 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1.50 | |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1.75 | |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 2.00 | |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 2.25 | |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 2.50 | |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 2.75 | |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 3.00 | |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 3.25 | 3.6 |
| | | | | | | | | ... | |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 5.25 | 5.4 |
| | | | | | | | | ... | |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 7.25 | 7.4 |
| | | | | | | | | ... | |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 9.25 | 9.4 |
| | | | | | | | | ... | |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 11.25 | 11.3 |
| | | | | | | | | ... | |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 13.25 | 13.3 |
| | | | | | | | | ... | |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 15.25 | 15.2 |
| | | | | | | | | ... | |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 17.25 | 17.3 |
| | | | | | | | | ... | |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 19.25 | 19.2 |
| | | | | | | | | ... | |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 21.25 | 21.2 |
| | | | | | | | | ... | |

| bBASS | | | | | | | | BASS USB HOST (dB) | BASS USB APRP (dB) |
|---|---|---|---|---|---|---|---|---|---|
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | | |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 23.25 | 23.2 |
| | | | | | | | | ... | |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 25.25 | 23.2 |
| | | | | | | | | ... | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 27.25 | 23.2 |
| | | | | | | | | ... | |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 29.25 | 23.2 |
| | | | | | | | | ... | |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 31.25 | 23.2 |
| | | | | | | | | ... | |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 31.75 | 23.2 |

### Dynamic bass boost control

Bass boost is one of the sound features as defined in the *"USB Device Class Definition for Audio Devices"*.
The bass boost control request data **bBassBoost** controls the position of the bass boost switch. The position can be either on or off. When **bBassBoost** is true the bass boost is activated. When **bBassBoost** is false the bass boost is off.

When clipping prevention is active, the bass is reduced to avoid clipping with high volume settings. Bass boost is selectable via the configuration map.

### Clipping prevention

When clipping prevention is ON and the sum of bass plus volume gives clipping, the bass is reduced. When clipping prevention is ON and the sum of treble plus volume gives clipping, the treble is reduced. Clipping prevention and clipping level are selectable via the configuration map. For more information about clipping prevention and the clipping level see the application documentation.

### De-emphasis

De-emphasis is one of the properties which is not supported by the USB. De-emphasis for 44.1 kHz can be predefined in the configuration map selected at start-up of the UDA1335H.

### Start-up and configuration of the UDA1335H

#### START-UP OF THE UDA1335H

After power-on, an internal power-on reset signal becomes HIGH after a certain RC time ($R = 5000\ \Omega$, $C = C_{ref}$). During 20 ms after power-on reset the UDA1335H has to initiate the internal settings. After the power-on reset the UDA1335H becomes master of the $I^2C$-bus.
The UDA1335H tries to read the eventually connected $I^2C$-bus EEPROM and if an dedicated EEPROM is detected, the internal descriptors are overwritten and the selected port configuration is applied. If no EEPROM is detected, the UDA1335H tries to read the logic levels of GP3 and GP4. A choice can be made from four configuration maps via these two GP pins.

#### CONFIGURATION SELECTION OF THE UDA1335H VIA A DIODE MATRIX

The UDA1335H uses a configuration map to hold a number of specific configurable data on hardware, product, component and USB configuration level.
At start-up, without EEPROM, the UDA1335H will scan the logic levels of GP3 and GP4. With these two GP pins it is possible to select one of the four possible configuration maps which are held in the external (E)PROM. This selection can be achieved via a diode matrix (see Fig.5).

After selecting an internal configuration map the user cannot change the chosen settings for the GP pins, internal configuration, descriptors etc.

The UDA1335H supports a maximum of two push-buttons (six with I²C-bus expanders), which represent a certain feature of the UDA1335H.

The UDA1335H supports a maximum of three outputs for e.g. user LEDs.

For more information about the four configuration maps located in the (E)PROM and the input and output functions of the UDA1335H see the application documentation.

### CONFIGURATION OPTIONS OF THE UDA1335H VIA AN I²C-BUS EEPROM

At start-up, the UDA1335H will address I²C-bus slave address 0 × A0H and will check the first two byte locations of the I²C-bus device with 0 × 55H and 0 × AAH. If a match occurs, the UDA1335H assumes that this I²C-bus device is an EEPROM which is dedicated to the UDA1335H. It will then read the configuration map stored in this EEPROM instead of one of four configuration maps located in the firmware of the microcontroller. The layout of the configuration map is fixed, the values (except bytes 0 and 1) are user definable. If the user wants to change e.g. the manufacturer name this can be achieved via the EEPROM code.

The communication between the UDA1335H and the external I²C-bus device is based on the standard I²C-bus protocol given in the Philips specification *"The I²C-bus and how to use it (including specifications)"*, which can be ordered using the code 9398 393 40011. The I²C-bus has two lines; a clock line SCL and a serial data line SDA (see Fig.6).

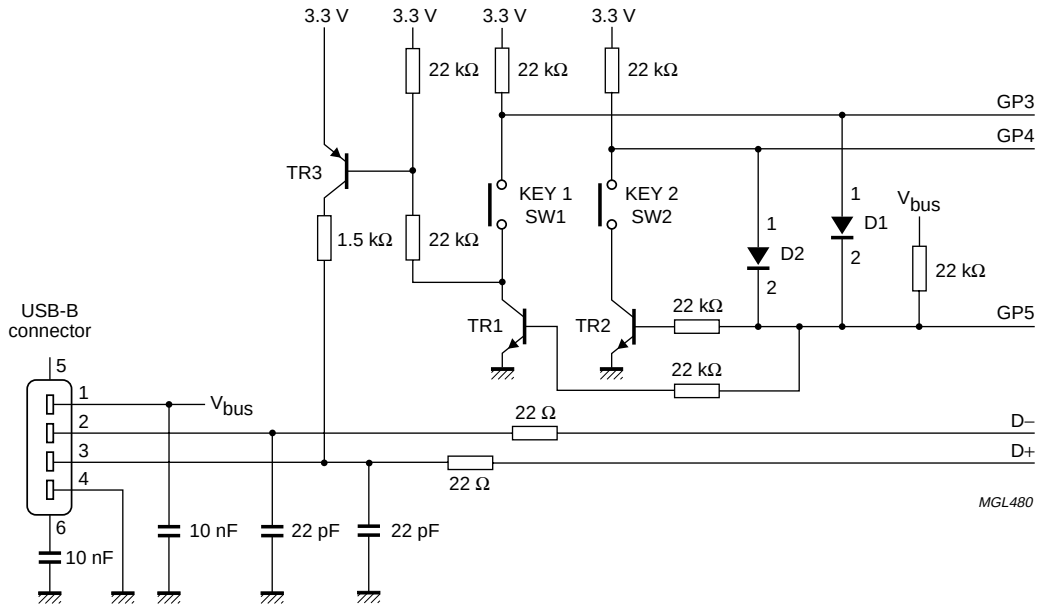



Fig.5 Diode matrix selection.

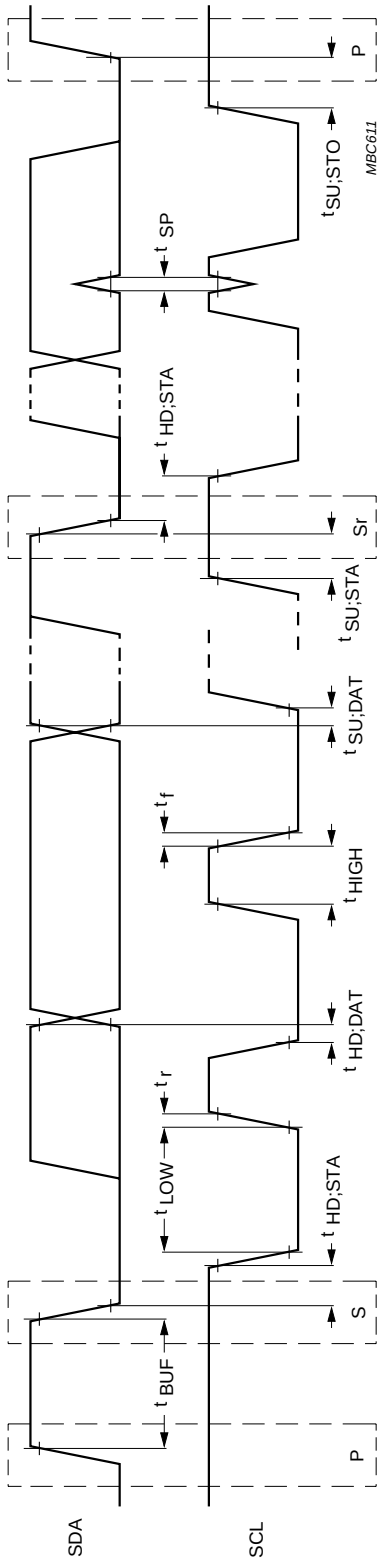



Fig.6 Definition of timing of the I²C-bus.

**Table 10** Control options for the UDA1335H via the EEPROM configuration map; note 1

| BYTE (HEX) | AFFECTS | COMMENTS | BIT | VALUE |
|---|---|---|---|---|
| 0 | | recognition pattern do not change it | | 55H |
| 1 | | recognition pattern do not change it | | AAH |
| 2 | clocks control register | selection ADC clock source | 7 | 0 = ADC clock from APLL |
| | | | | 1 = ADC clock from OSCAD |
| | | divide factor | 6 and 5 | 00 = ADC clock divided-by-1 |
| | | | | 01 = ADC clock divided-by-2 |
| | | | | 10 = ADC clock divided-by-4 |
| | | | | 11 = ADC clock divided-by-8 |
| | | clock ADAC | 4 | 0 |
| | | clock 48 MHz internal | 3 | 0 |
| | | clock recovered PSIE/MMU | 2 | 0 |
| | | ADC clock | 1 | 0 |
| | | power on OSCAD | 0 | 0 |
| 3 | reset generator and APLL control register | | | 00H |
| 4 | power control register analog modules | | | 00H |
| 5 | ASR control register | robust word clock | 7 | 1 |
| | | serial $I^2S$-bus output format | 6 and 5 | 00 = $I^2S$-bus |
| | | | | 01 = 16-bit LSB |
| | | | | 10 = 18-bit LSB |
| | | | | 11 = 20-bit LSB |
| | | phase inversion (right output) | 4 | 0 = mono phase inversal off |
| | | | | 1 = mono phase inversal on |
| | | bits per sample modi | 3 and 2 | 00 = reserved |
| | | | | 01 = 8-bit audio |
| | | | | 10 = 16-bit audio |
| | | | | 11 = 24-bit audio |
| | | mono or stereo operation | 1 | 0 = mono |
| | | | | 1 = stereo |
| | | ASR register start-up mode | 0 | 1 |

| BYTE (HEX) | AFFECTS | COMMENTS | BIT | VALUE |
|---|---|---|---|---|
| 6 | PGA control register input terminal 1 (all analog input topologies) | reserved | 7 | X |
| | | PGA internal setting (do not change it) | 6 | 0 |
| | | PGA gain selection right channel | 5 to 3 | 000 = –3 dB |
| | | | | 001 = 0 dB |
| | | | | 010 = 3 dB |
| | | | | 011 = 9 dB |
| | | | | 100 = 15 dB |
| | | | | 101 = 21 dB |
| | | | | 110 = 27 dB |
| | | | | 111 = 27 dB |
| | | PGA gain selection left channel | 2 to 0 | 000 = –3 dB |
| | | | | 001 = 0 dB |
| | | | | 010 = 3 dB |
| | | | | 011 = 9 dB |
| | | | | 100 = 15 dB |
| | | | | 101 = 21 dB |
| | | | | 110 = 27 dB |
| | | | | 111 = 27 dB |
| 7 | PGA control register input terminal 2 (only for analog input topology 2) | reserved | 7 | X |
| | | PGA internal setting (do not change it) | 6 | 0 |
| | | PGA gain selection right channel | 5 to 3 | 000 = –3 dB |
| | | | | 001 = 0 dB |
| | | | | 010 = 3 dB |
| | | | | 011 = 9 dB |
| | | | | 100 = 15 dB |
| | | | | 101 = 21 dB |
| | | | | 110 = 27 dB |
| | | | | 111 = 27 dB |
| | | PGA gain selection left channel | 2 to 0 | 000 = –3 dB |
| | | | | 001 = 0 dB |
| | | | | 010 = 3 dB |
| | | | | 011 = 9 dB |
| | | | | 100 = 15 dB |
| | | | | 101 = 21 dB |
| | | | | 110 = 27 dB |
| | | | | 111 = 27 dB |

| BYTE (HEX) | AFFECTS | COMMENTS | BIT | VALUE |
|---|---|---|---|---|
| 8 | ADIF control register | reserved | 7 | X |
| | | number of bits per audio sample to be transmitted to the host | 6 and 5 | 00 = reserved |
| | | | | 01 = 8 bits audio samples |
| | | | | 10 = 16 bits audio samples |
| | | | | 11 = 24 bits audio samples |
| | | mono/stereo selection | 4 | 0 = mono |
| | | | | 1 = stereo |
| | | selection audio input channel | 3 | 0 = digital serial audio input |
| | | | | 1 = analog input |
| | | selection high-pass filter of the decimation module | 2 | 0 = high-pass filter off |
| | | | | 1 = high-pass filter on |
| | | $I^2S$-bus input serial input format | 1 and 0 | 00 = $I^2S$-bus |
| | | | | 01 = 16-bit LSB |
| | | | | 10 = 18-bit LSB |
| | | | | 11 = 20-bit LSB |
| 9 | ADAC feature setting register | selection ADAC mode register | 7 | 0 |
| | | audio feature mode | 6 and 5 | 11 |
| | | de-emphasis | 4 | 0 = de-emphasis off |
| | | | | 1 = de-emphasis on |
| | | channel manipulation | 3 | 0 = L $\rightarrow$ L, R $\rightarrow$ R |
| | | | | 1 = L $\rightarrow$ R, R $\rightarrow$ L |
| | | synchronous/asynchronous | 2 | 0 |
| | | mute control | 1 | 1 |
| | | reset ADAC | 0 | 0 |
| A | ADAC lock mode register | selection ADAC mode register | 7 | 1 |
| | | digital PLL lock speed | 6 and 5 | 00 |
| | | digital PLL lock mode | 4 | 1 |
| | | digital PLL mode | 3 and 2 | 00 |
| | | serial $I^2S$-bus input format | 1 and 0 | 00 = $I^2S$-bus |
| | | | | 01 = 16-bit LSB |
| | | | | 10 = 18-bit LSB |
| | | | | 11 = 20-bit LSB |

| BYTE (HEX) | AFFECTS | COMMENTS | BIT | VALUE |
|---|---|---|---|---|
| B | I/O selection register | clipping | 7 | 0 = clipping prevention OFF |
| | | | | 1 = clipping prevention ON |
| | | expander | 6 | 0 = no $I^2C$-bus expander used |
| | | | | 1 = $I^2C$-bus expander used |
| | | selector output (GP2) | 5 | 0 = selector state normal |
| | | | | 1 = selector state inverted |
| | | mute/standby expander | 4 | 0 = mute |
| | | | | 1 = standby |
| | | mute/standby USB APRP | 3 | 0 = mute |
| | | | | 1 = standby |
| | | output pin 3 | 2 | polarity output pins |
| | | output pin 2 | 1 | 0 = inverted logic |
| | | output pin 1 | 0 | 1 = normal logic |
| C | | output pin function 1 | | functions are available if declared in ADC: 0 = mute LED; 1 = DBB LED |
| D | | output pin function 2 | | |
| E | | output pin function 3 | | |
| F | $I^2S$-bus and topology selection register | output $I^2S$-bus | 7 | 0 = no $I^2S$-bus used |
| | | | | 1 = $I^2S$-bus used |
| | | 4-pin or 6-pin $I^2S$-bus | 6 | only if $I^2S$-bus is used: 0 = 4-pin $I^2S$-bus 1 = 6-pin $I^2S$-bus |
| | | HID usage | 5 | 0 = HID not included |
| | | | | 1 = HID included |
| | | reserved | 4 | X |
| | | topology selection | 3 | low nibble: 1 = input topology 1 2 = input topology 2 3 = input topology 3 4 = input topology 4 all other values = input topology 1 |
| | | | 2 | |
| | | | 1 | |
| | | | 0 | |
| 10 | | rise time power amplifier, steps of 20 ms | | |
| 11 | | time between mute and play, steps of 1 s | | |
| 12 | | time between mute and standby, steps of 5 s | | |
| 13 | | selector preferred state (only applicable in input topology 2) | | 0 = terminal Input 1 or terminal input 2 |
| 14 | | DBB value steps of 1 dB with maximum 255 dB | | 0 = no DBB active |
| | | | | 1 to FF = DBB active |
| 15 | | start-up volume value in dB | | volume = –register value |

| BYTE (HEX) | AFFECTS | COMMENTS | BIT | VALUE |
|---|---|---|---|---|
| 16 | | maximum distortion in dB | | |
| 17 | sample frequency | LSB | | |
| 18 | | mid | | |
| 19 | | MSB | | |
| 1A/1B | | pointer to device descriptor | | 0030 |
| 1C/1D | | pointer to configuration descriptor | | 0045 |
| 1E/1F | | pointer to HID descriptor | | 01F0 |
| 20/21 | | pointer to HID report descriptor | | 0210 |
| 22 | | number of string pointers (N + 1) maximum for N is 31 | | |
| 23/24 | | pointer to string 0 | | 025E |
| 25/26 | | pointer to string 1 | | 0260 |
| 27/28 | | pointer to string 2 | | 0290 |
| 29/2A | | pointer to string 3 | | 02D0 |
| : | | : | | |
| 23 + 2N/ 24 + 2N | | pointer to string N | | |
| 30 → | | device descriptor | | |
| 45 →<br><br>1F0 → | | configuration descriptor including ADC<br><br>and HID descriptors | | 32 |
| 210 →<br><br>212 → | | wDescriptorLength<br><br>HID report descriptor | | |
| 25E → | string 0 | language string | | |
| 260 → | string 1 | manufacturer string | | |
| 290 → | string 2 | product string | | |
| 2D0 → | string 3 | serial number(2) | | |

**Notes**

1. An extensive description of the USB control options is available in the *"USB Device Class Definition for Audio Devices"*.
2. The serial number is only supported in the external configuration map and not in the four internal configuration maps.

### The general purpose I/O pins (GP0 to GP5) and I²C-bus expander option

The UDA1335H has 6 General Purpose (GP) I/O pins; these are pins GP0 to GP5. These can be used either for digital I/O functions or for general purposes.

There are basically three port configurations:

- No digital I/O communication
- 4-pin digital I/O communication
- 6-pin digital I/O communication.

These port configurations can be chosen via the configuration map at start-up of the UDA1335H.

The user can also make use of an I²C-bus expander. The usage of an I²C-bus expander (yes/no) can be indicated via the configuration map. Some of the supported HID functions are located in the I²C-bus expander. If this expander is not used, the HID functions normally located in the expander must be declared as “unassigned” in the HID report descriptor. The bit which indicates if an external expander is used must then be put on zero.

**Table 11** Definition of the general purpose pins and I²C-bus expander pins; notes 1 to 6

| PINS | NO I²S-BUS USAGE | 4-PIN I²S-BUS USAGE | 6-PIN I²S-BUS USAGE |
|---|---|---|---|
| **General purpose I/O** | | | |
| GP5 | connect/disconnect | connect/disconnect | WS input |
| GP4 | HID input 2 | BCK output | BCK output |
| GP3 | HID input 1 | WS output | WS output |
| GP2 | selector output | DATA output | DATA output |
| GP1 | mute or standby output | DATA input | DATA input |
| GP0 | interrupt input | interrupt input | BCK input |
| **I²C-bus expander;** note 7 | | | |
| P0 | HID input 3 | HID input 3 | connect/disconnect |
| P1 | HID input 4 | HID input 4 | HID input 4 |
| P2 | HID input 5 | HID input 5 | HID input 5 |
| P3 | HID input 6 | HID input 6 | HID input 6 |
| P4 | output pin 1 | output pin 1 | output pin 1 |
| P5 | output pin 2 | output pin 2 | output pin 2 |
| P6 | output pin 3 | selector output | selector output |
| P7 | mute or standby output | mute or standby output | mute or standby output |

**Notes**

1. Connect/disconnect: This pin can be used to avoid malfunction during initialisation phase of the UDA1335H. While initialization takes place, the USB can be kept disconnected while the software of the microcontroller reads in the configuration map. When the UDA1335H is ready, the USB becomes connected and enumeration can start. Using the 6-pin I²S-bus, the connect/disconnect will be moved to the I²C-bus expander.
2. HID input 1 to 6 and interrupt input: A change on the expander can be signalled to the UDA1335H via the interrupt input. After detecting this signal the UDA1335H will decode the buttons. When no expander is used, the interrupt pin must be connected to the ground. The HID input pins and the interrupt input pin on the UDA1335H are scanned each 20 ms. If the interrupt in pin indicates a change on the expander, the expander input pins are scanned once. Using the 6-pin I²S-bus, the interrupt pin is not available and the inputs on the expander are scanned every 20 ms. All input pins must have a pull-up resistor.
3. Selector output: This pin can be used for switching the audio selector as illustrated in Fig.4. If the configuration map does not request this output pin, the output is always LOW.
4. Mute output: This output is activated if the isochronous signal is not available during a certain time. The output levels and the time are programmable in the configuration map.
5. Standby output: This output is activated if the UDA1335H is muted during a certain time. The output levels and the time are programmable in the configuration map.
6. Output pins 1 to 3: All the output pins are set via the I²C-bus. The function is according the configuration map.
7. For the I²C-bus expander, the PCF8574P remote 8-bit I/O expander for I²C-bus can be used.

**Filter characteristics**

The overall filter characteristic of the UDA1335H in flat mode is given in the Fig.7. The overall filter characteristic of the UDA1335H includes the filter characteristics of the DSP in flat mode plus the filter characteristic of the FSDAC ($f_s$ = 44.1 kHz)

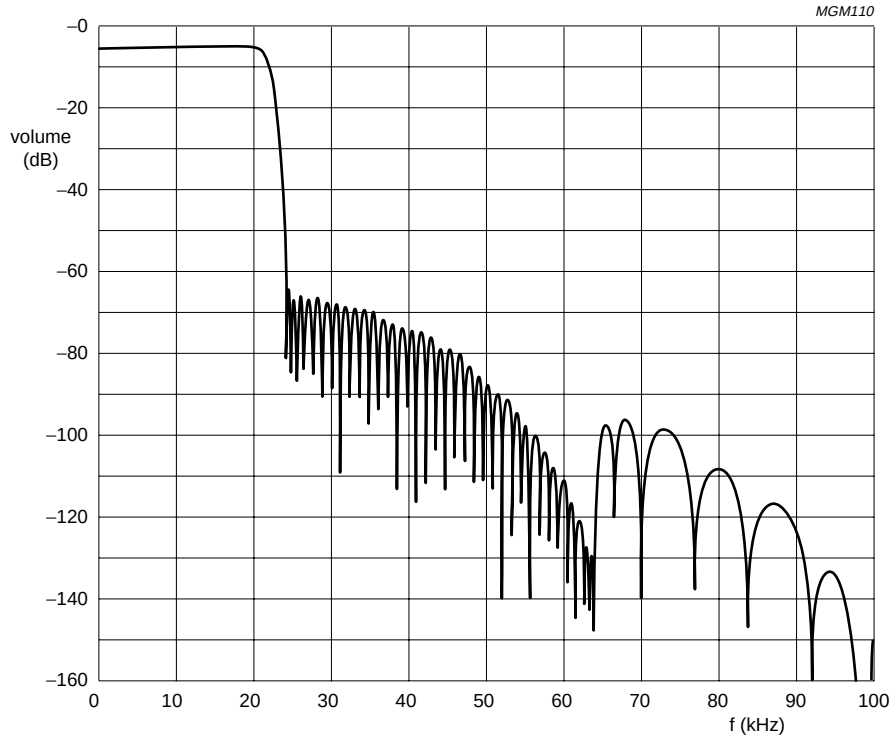



Fig.7 Overall filter characteristics of the UDA1335H.

**DSP extension port**

An external DSP can be used for adding extra sound processing features via the digital I/O-bus. The UDA1335H supports the standard $I^2S$-bus data protocol and the LSB-justified serial data input format with word lengths of 16, 18 and 20 bits. Using the 4-pin digital I/O-bus the UDA1335H device acts as a master, controlling the BCK and WS signals.

The period of the WS signal is determined by the number of samples in the 1 ms frame of the USB. This implies that the WS signal does not have a constant time period, but is jittery. Using the 6-pin digital I/O-pins GP2, GP3 and GP4 are output pins (master) and GP0, GP1 and GP5 are input pins (slave).

The characteristic timing of the $I^2S$-bus input interface is illustrated in Figs 8 and 9.

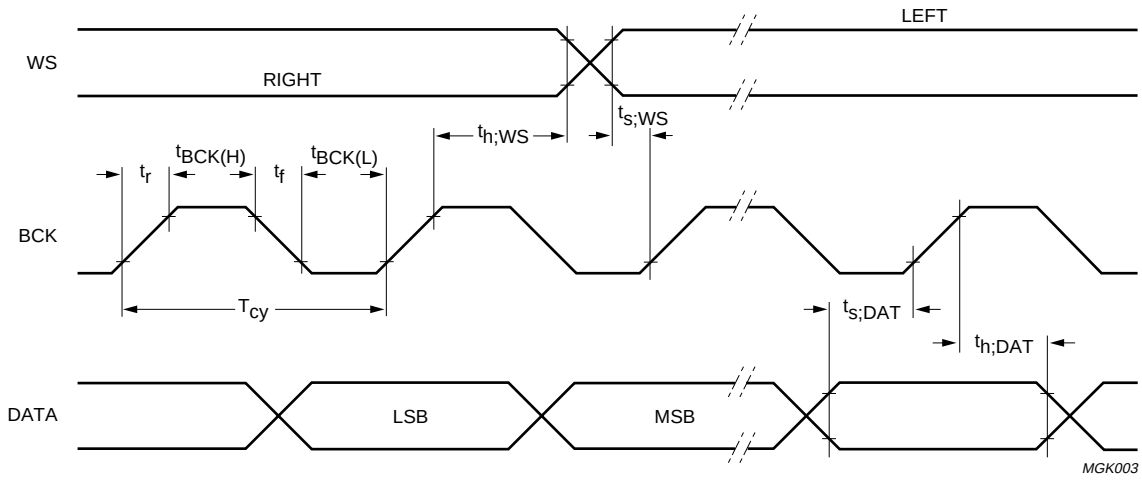



Fig.8 Timing of digital I/O input signals.

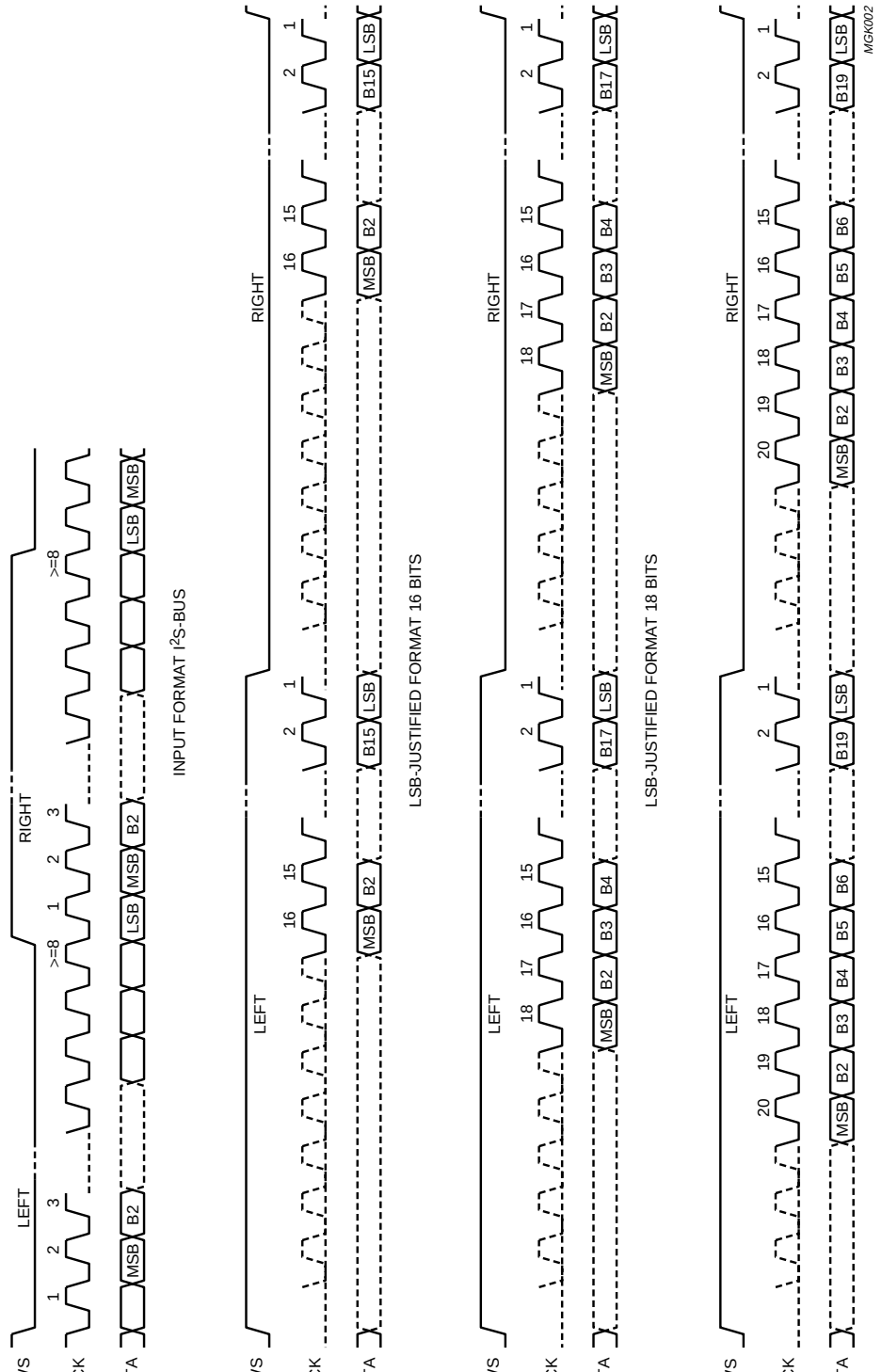



Fig.9 Input formats.

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **All digital I/Os** | | | | | | |
| $V_{I/O}$ | DC input/output voltage range | | –0.5 | – | $V_{DDE}$ | V |
| $I_O$ | output current | $V_{DDE}$ = 5.0 V | – | – | 4 | mA |
| **Temperature values** | | | | | | |
| $T_j$ | junction temperature | | 0 | – | 125 | °C |
| $T_{stg}$ | storage temperature | | –55 | – | +150 | °C |
| $T_{amb}$ | operating ambient temperature | | 0 | 25 | 70 | °C |
| **Electrostatic handling** | | | | | | |
| $V_{es}$ | electrostatic handling | note 1 | –3000 | – | +3000 | V |
| | | note 2 | –300 | – | +300 | V |

**Notes**

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
2. Equivalent to discharging a 200 pF capacitor through a 2.5 μH series conductor.

## THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| $R_{thj-a}$ | thermal resistance from junction to ambient | in free air | 48 | K/W |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{DDE}$ | supply voltage periphery (I/O) | 4.75 | 5.0 | 5.25 | V |
| $V_{DD}$ | supply voltage (core) | 3.0 | 3.3 | 3.6 | V |
| $V_I$ | DC input voltage range | | | | |
| | for D+ and D– | 0.0 | – | $V_{DD}$ | V |
| | for VINL and VINR | – | $0.5V_{DD}$ | – | V |
| | for digital I/Os | 0.0 | – | $V_{DDE}$ | V |

**DC CHARACTERISTICS**

$V_{DDE}$ = 5.0 V; $V_{DD}$ = 3.3 V; $T_{amb}$ = 25 °C; $f_{osc}$ = 48 MHz; $f_s$ = 44.1 kHz; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Supplies** | | | | | | |
| $V_{DDE}$ | digital supply voltage periphery | | 4.75 | 5.0 | 5.25 | V |
| $V_{DDI}$ | digital supply voltage core | | 3.0 | 3.3 | 3.6 | V |
| $V_{DDA1}$ | analog supply voltage 1 | | 3.0 | 3.3 | 3.6 | V |
| $V_{DDA2}$ | analog supply voltage 2 | | 3.0 | 3.3 | 3.6 | V |
| $V_{DDA3}$ | analog supply voltage 3 | | 3.0 | 3.3 | 3.6 | V |
| $V_{DDO}$ | operational amplifier supply voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_{DDX}$ | crystal oscillator supply voltage | | 3.0 | 3.3 | 3.6 | V |
| $I_{DDE}$ | digital supply current periphery | note 1 | – | 3.7 | – | mA |
| $I_{DDI}$ | digital supply current core | | – | 39.0 | – | mA |
| $I_{DDA1}$ | analog supply current 1 | | – | 3.6 | – | mA |
| $I_{DDA2}$ | analog supply current 2 | | – | 8.0 | – | mA |
| $I_{DDA3}$ | analog supply current 3 | | – | 0.9 | 9.0[2] | mA |
| $I_{DDO}$ | operational amplifier supply current | | – | 3.0 | – | mA |
| $I_{DDX}$ | crystal oscillator supply current | | – | 1.2 | 13.0[3] | mA |
| $P_{tot}$ | total power dissipation | | – | 200 | – | mW |
| $P_{ps}$ | total power dissipation in power saving mode | note 4 | – | 1.2 | – | mW |
| **Inputs/outputs D+ and D–** | | | | | | |
| $V_I$ | static DC input voltage | | –0.5 | – | $V_{DDI}$ | V |
| $V_{O(H)}$ | static DC output voltage HIGH | $R_L$ = 15 kΩ connected to GND | 2.8 | – | 3.6 | V |
| $V_{O(L)}$ | static DC output voltage LOW | $R_L$ = 15 kΩ connected to $V_{DD}$ | – | – | 0.3 | V |
| $\lvert I_{LO} \rvert$ | high impedance data line output leakage current | | – | – | 10 | μA |
| $V_{I(diff)}$ | differential input sensitivity | | 0.2 | – | – | V |
| $V_{CM(diff)}$ | differential common mode range | | 0.8 | – | 2.5 | V |
| $V_{SE(R)(th)}$ | single-ended receiver threshold voltage | | 0.8 | – | 2.0 | V |
| $C_{IN}$ | transceiver input capacitance | pin to GND | – | – | 20 | pF |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Digital input pins** | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | – | – | $0.3V_{DDE}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | $0.7V_{DDE}$ | – | $V_{DDE}$ | V |
| $\|I_{LI}\|$ | input leakage current | | – | – | 1 | μA |
| $C_I$ | input capacitance | | – | – | 5 | pF |
| **PGA and ADC** | | | | | | |
| $V_{ref(AD)}$ | reference voltage PGA and ADC | | – | $0.5V_{DDA2}$ | – | V |
| $V_{ref(ADC)(pos)}$ | positive reference voltage of the ADC | | – | $V_{DDA2}$ | – | V |
| $V_{ref(ADC)(neg)}$ | negative reference voltage of the ADC | | – | 0.0 | – | V |
| $V_{I(PGA)}$ | DC input voltage VINL and VINR of the PGA | | – | $0.5V_{DDA2}$ | – | V |
| $R_{I(PGA)}$ | DC input resistance at VINL and VINR of the PGA | | – | 12.5 | – | kΩ |
| **Filter stream DAC** | | | | | | |
| $V_{ref(DA)}$ | reference voltage DAC | | – | $0.5V_{DDA1}$ | – | V |
| $V_{O(CM)}$ | common mode output voltage | | – | $0.5V_{DDA1}$ | – | V |
| $R_{O(VOUT)}$ | output resistance at VOUTL and VOUTR | | – | 11 | – | Ω |
| $R_{O(L)}$ | output load resistance | | 2.0 | – | – | kΩ |
| $C_{O(L)}$ | output load capacitance | | – | – | 50 | pF |

**Notes**

1. This value depends strongly on the application. The specified value is the typical value obtained using the application diagram as illustrated in Fig.10.
2. At start-up of the OSCAD oscillator.
3. At start-up of the OSC48 oscillator.
4. Exclusive the $I_{DDE}$ current which depends on the components connected to the I/O pins.

**AC CHARACTERISTICS**

$V_{DDE}$ = 5.0 V; $V_{DDI}$ = 3.3 V; $T_{amb}$ = 25 °C; $f_{osc}$ = 48 MHz; $f_s$ = 44.1 kHz; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Driver characteristics D+ and D- (full-speed mode)** | | | | | | |
| $f_{o(s)}$ | audio sample output frequency | | 5 | – | 55 | kHz |
| $t_r$ | rise time | $C_L$ = 50 pF | 4 | – | 20 | ns |
| $t_f$ | fall time | $C_L$ = 50 pF | 4 | – | 20 | ns |
| $t_{rf(m)}$ | rise/fall time matching ($t_r/t_f$) | | 90 | – | 110 | % |
| $V_{cr}$ | output signal crossover voltage | | 1.3 | – | 2.0 | V |
| $R_{o(drive)}$ | driver output resistance | steady-state drive | 28 | – | 43 | Ω |
| **Data source timings D+ and D- (full-speed mode)** | | | | | | |
| $f_{i(s)}$ | audio sample input frequency | | 5 | – | 55 | kHz |
| $f_{fs(D)}$ | full speed data rate | | 11.97 | 12.00 | 12.03 | Mbits/s |
| $t_{fr(D)}$ | frame interval | | 0.9995 | 1.0000 | 1.0005 | ms |
| $t_{J1(diff)}$ | source differential jitter to next transition | | −3.5 | +0.0 | +3.5 | ns |
| $t_{J2(diff)}$ | source differential jitter for paired transitions | | −4.0 | +0.0 | +4.0 | ns |
| $t_{W(EOP)}$ | source end of packet width | | 160 | – | 175 | ns |
| $t_{EOP(diff)}$ | differential to end of packet transition skew | | −2.0 | – | +5.0 | ns |
| $t_{JR1}$ | receiver data jitter tolerance to next transition | | −18.5 | 0.0 | +18.5 | ns |
| $t_{JR2}$ | receiver data jitter tolerance for paired transitions | | −9.0 | 0.0 | +9.0 | ns |
| $t_{EOPR1}$ | end of packet width at receiver must reject as end of packet | | 40 | – | – | ns |
| $t_{EOPR2}$ | end of packet width at receiver must accept as end of packet | | 82 | – | – | ns |
| **Serial input/output data timing** | | | | | | |
| $f_s$ | system clock frequency | | – | 12 | – | MHz |
| $f_{i(WS)}$ | word selection input frequency | | 5 | – | 55 | kHz |
| $t_r$ | rise time | | – | – | 20 | ns |
| $t_f$ | fall time | | – | – | 20 | ns |
| $t_{BCK(H)}$ | bit clock HIGH time | | 55 | – | – | ns |
| $t_{BCK(L)}$ | bit clock LOW time | | 55 | – | – | ns |
| $t_{s;DAT}$ | data set-up time | | 10 | – | – | ns |
| $t_{h;DAT}$ | data hold time | | 20 | – | – | ns |
| $t_{s;WS}$ | word selection set-up time | | 20 | – | – | ns |
| $t_{h;WS}$ | word selection hold time | | 10 | – | – | ns |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **SDA and SCL lines (standard mode $I^2C$-bus)** | | | | | | |
| $f_{SCL}$ | SCL clock frequency | | 0 | – | 100 | kHz |
| $t_{BUF}$ | bus free time between a STOP and START condition | | 4.7 | – | – | µs |
| $t_{HD;STA}$ | hold time (repeated) START condition | | 4.0 | – | – | µs |
| $t_{LOW}$ | LOW period of the SCL clock | | 4.7 | – | – | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | | 4.0 | – | – | µs |
| $t_{SU;STA}$ | set-up time for a repeated START condition | | 4.7 | – | – | µs |
| $t_{SU;STO}$ | set-up time for STOP condition | | 4.0 | – | – | µs |
| $t_{HD;DAT}$ | data hold time | | 5.0 | – | 0.9 | µs |
| $t_{SU;DAT}$ | data set-up time | | 250 | – | – | ns |
| $t_r$ | rise time of both SDA and SCL signals | | – | – | 1000 | ns |
| $t_f$ | fall time of both SDA and SCL signals | | – | – | 300 | ns |
| $C_{L(bus)}$ | capacitive load for each bus line | | – | – | 400 | pF |
| **Oscillator 1 (system clock)** | | | | | | |
| $f_{osc}$ | oscillator frequency | | – | 48 | – | MHz |
| $\delta$ | duty factor | | – | 50 | – | % |
| $g_m$ | transconductance | | 12.8 | 22.1 | 30.2 | mS |
| $R_o$ | output resistance | | 0.6 | 1.1 | 2.3 | kΩ |
| $C_{i(XTAL1a)}$ | parasitic input capacitance XTAL1a | | 4.5 | 4.8 | 5.2 | pF |
| $C_{i(XTAL2a)}$ | parasitic input capacitance XTAL2a | | 4.1 | 4.6 | 5.0 | pF |
| $I_{start}$ | start-up current | | 3.7 | 7.6 | 13.0 | mA |
| **Oscillator 2 (for ADC clock)** | | | | | | |
| $f_{osc}$ | oscillator frequency | | 8.192 | – | 14.08 | MHz |
| $\delta$ | duty cycle | | – | 50 | – | % |
| $g_m$ | transconductance | | 8.1 | 13.6 | 18.1 | mA/V |
| $R_o$ | output resistance | | 1.3 | 2.0 | 4.0 | kΩ |
| $C_{i(XTAL1b)}$ | parasitic input capacitance XTAL1b | | 5.0 | 5.4 | 5.7 | pF |
| $C_{i(XTAL2b)}$ | parasitic input capacitance XTAL2b | | 4.1 | 4.6 | 5.0 | pF |
| $I_{start}$ | start-up current | | 2.4 | 5.0 | 8.4 | mA |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Analog PLL (for ADC clock)** | | | | | | |
| $f_{clk(PLL)}$ | PLL clock frequency | | 8.1920 | 11.2896 | 12.2880 | MHz |
| $\delta$ | duty factor | | – | 50 | – | % |
| $t_{strt(PO)}$ | start-up time after power-on | | – | – | 10 | ms |
| **Power-on reset** | | | | | | |
| $t_{su(PO)}$ | power-on set-up-time | note 1 | $5C_{ref}$[2] | – | – | ms |
| **PGA and ADC** | | | | | | |
| $V_{i(FS)(rms)}$ | full-scale input voltage (RMS value) | PGA gain = –3 dB | – | 1414[5] | – | mV |
| | | PGA gain = 0 dB | – | 1000 | – | mV |
| | | PGA gain = 3 dB | – | 708 | – | mV |
| | | PGA gain = 9 dB | – | 355 | – | mV |
| | | PGA gain = 15 dB | – | 178 | – | mV |
| | | PGA gain = 21 dB | – | 89 | – | mV |
| | | PGA gain = 27 dB | – | 44 | – | mV |
| $C_{i(PGA)}$ | input capacitance of the PGA | | – | – | 20 | pF |
| (THD + N)/S | total harmonic distortion plus noise-to-signal ratio | $f_s$ = 44.1 kHz at input signal of 1 kHz; PGA gain = 0 dB; note 3 | | | | |
| | | $V_i$ (0 dB) (1.0 V RMS) | – | –85 | –80 | dB |
| | | | – | 0.0056 | 0.01 | % |
| | | $V_i$ (–60 dB) | – | –30 | –20 | dB |
| | | | – | 3.2 | 10.0 | % |
| S/N | signal to noise ratio | $V_i$ = 0.0 V | 90 | 95 | – | dBA |
| $\alpha_{ct}$ | crosstalk between channels | PGA gain = 0 dB | – | 100 | – | dB |
| $f_s$ | sample frequency ($128f_s$) | | 0.640 | – | 7.04 | MHz |
| $OL_{(FS)}$ | full-scale digital output level | PGA gain = 0 dB; $V_i$ = 1 V (RMS) | – | –2.0 | – | dB |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Filter stream DAC** | | | | | | |
| RES | resolution | | 16 | – | – | bits |
| $V_{o(FS)(rms)}$ | full-scale output voltage (RMS value) | $V_{DD}$ = 3.3 V | – | 0.66 | – | V |
| SVRR | supply voltage ripple rejection at $V_{DDA}$ and $V_{DDO}$ | $f_{ripple}$ = 1 kHz; $V_{ripple(p-p)}$ = 0.1 V | – | 60 | – | dB |
| $\lvert\Delta V_o\rvert$ | channel unbalance | maximum volume | – | 0.03 | – | dB |
| $\alpha_{ct}$ | crosstalk between channels | $R_L$ = 5 kΩ | – | 95 | – | dB |
| (THD + N)/S | total harmonic distortion plus noise-to-signal ratio | $f_s$ = 44.1 kHz; $R_L$ = 5 kΩ; note 4 | | | | |
| | | at input signal of 1 kHz (0 dB) | – | –90 | –80 | dB |
| | | | – | 0.0032 | 0.01 | % |
| | | at input signal of 1 kHz (–60 dB) | – | –30 | –20 | dB |
| | | | – | 3.2 | 10 | % |
| S/N | signal-to-noise ratio at bipolar zero | A-weighting at code 0000H | 90 | 95 | – | dB |

**Notes**

1. Strongly depends on the external decoupling capacitor connected to $V_{ref(DA)}$.
2. $C_{ref}$ in μF.
3. Measured with the APLL as ADC clock source.
4. Measured with $I^2S$-bus input as digital source.
5. Although a level of 1.414 V (RMS) would be required to optimal drive the ADC in this gain setting, this level can not be used. Due to the 3.3 V supply voltage input, signals of 1.17 V (RMS) and higher will result in clipping.

## APPLICATION INFORMATION

The UDA1335H can only be used in combination with an external (E)PROM. This (E)PROM can be connected to the port pins (P0 and P2) of the UDA1335H and must contain the firmware for the microcontroller. The UDA1335H will be delivered with standard USB compliant firmware. The $I^2C$-bus EEPROM is optional and can be used to configure client specific configurations and descriptors.

More information about the firmware, descriptors and configurations can be obtained from several application notes.

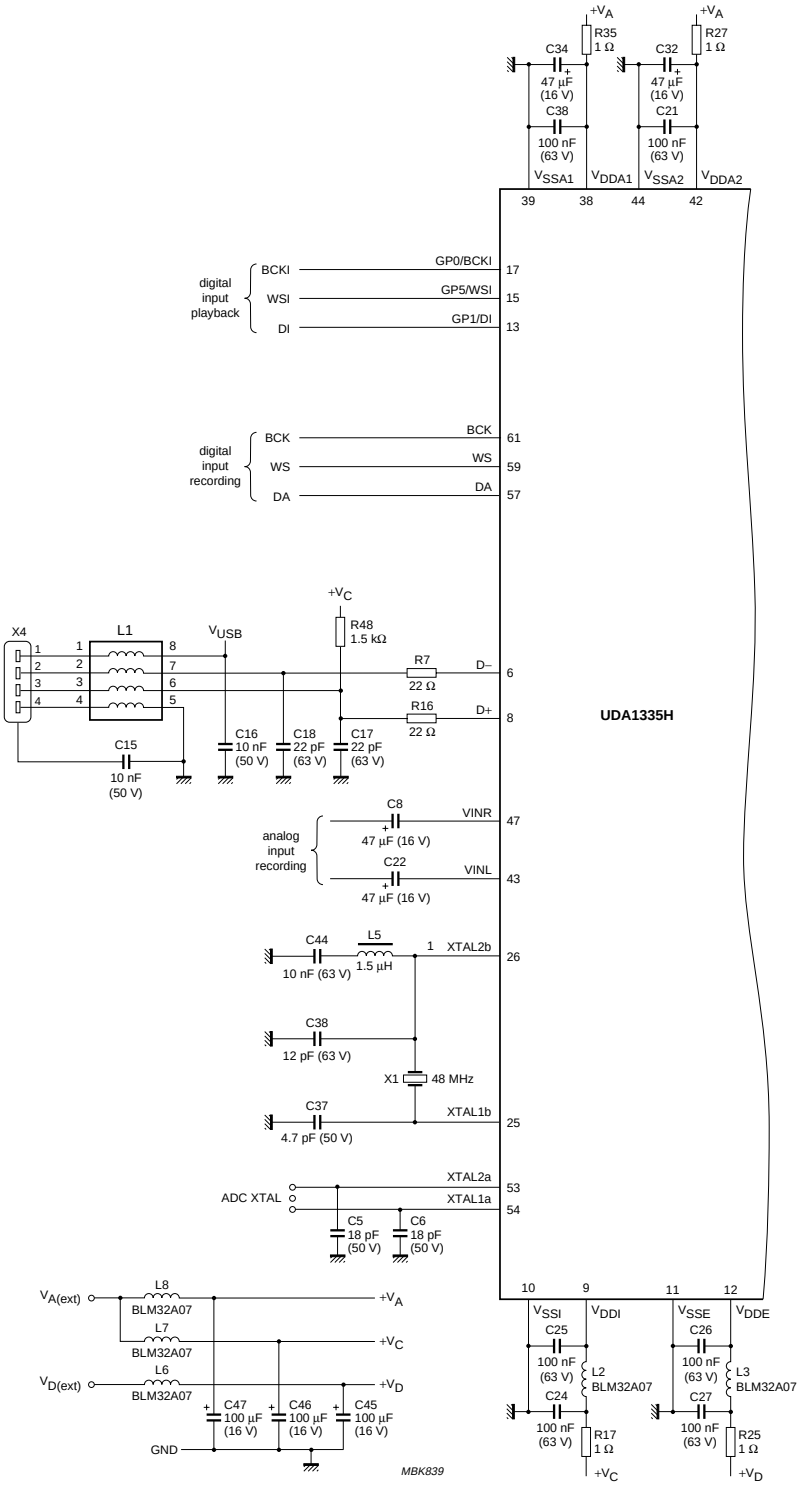



Fig.10 Application diagram (continued in Fig.11).

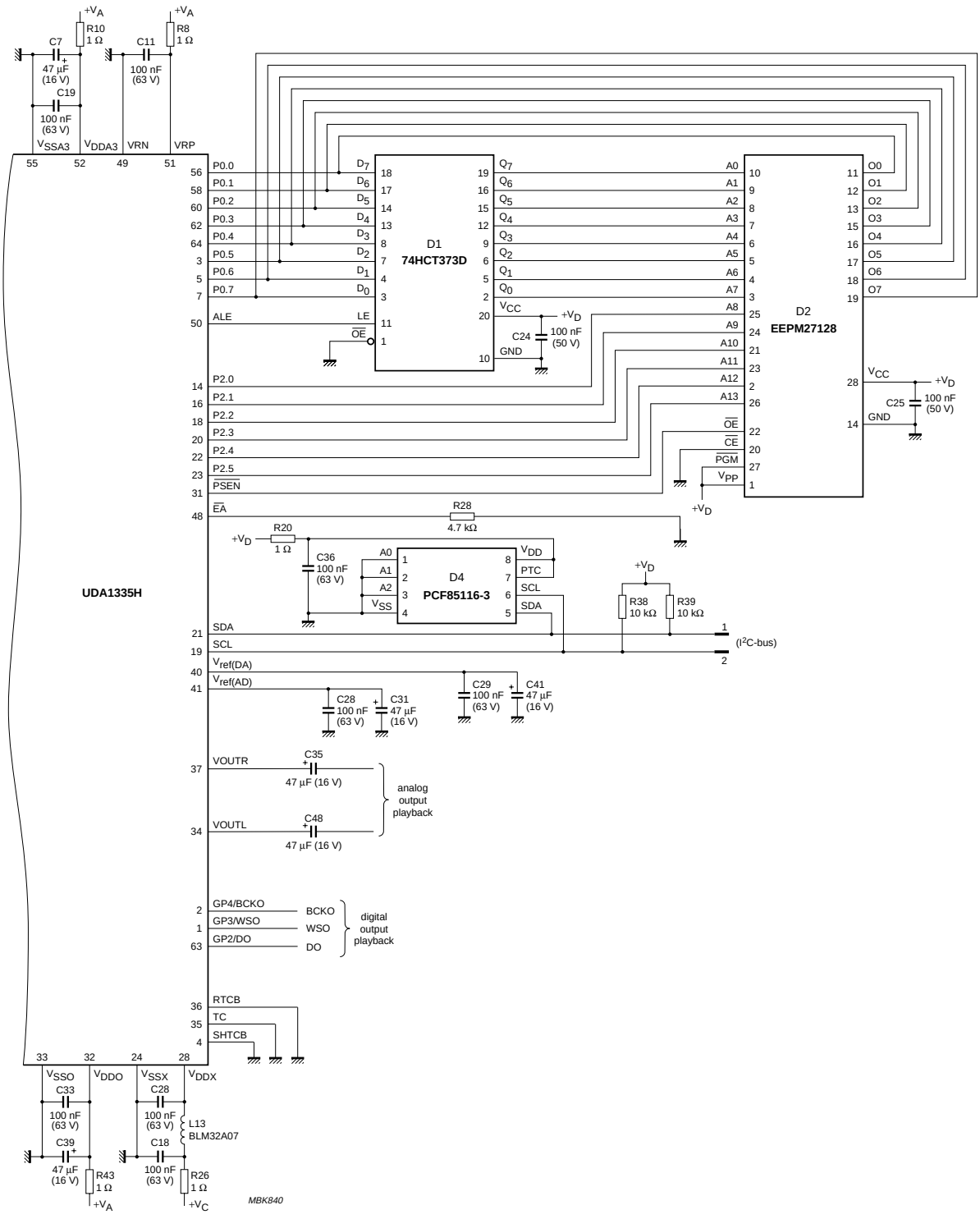
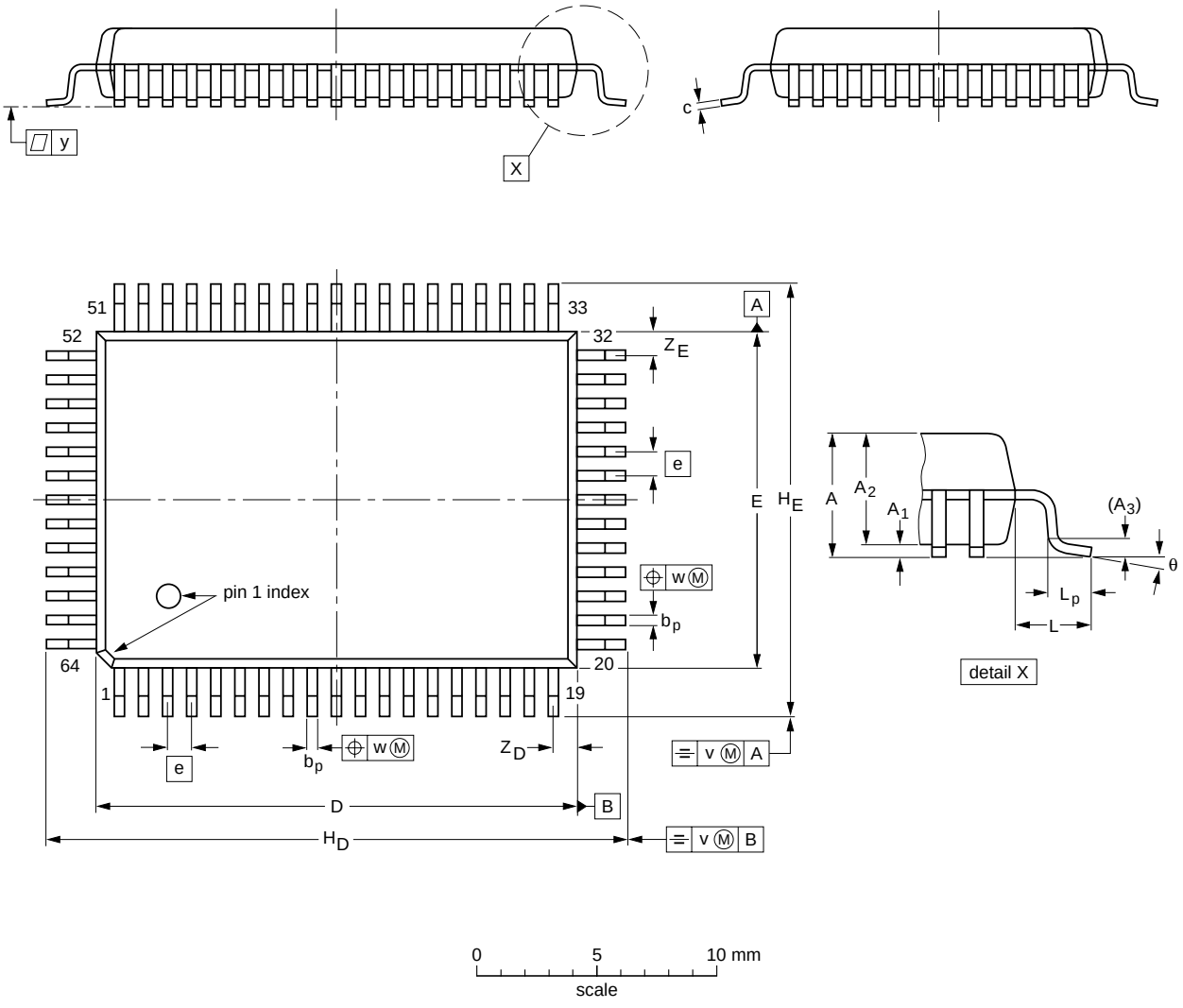



Fig.11 Application diagram (continued from Fig.10).

## PACKAGE OUTLINE

**QFP64: plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm** **SOT319-2**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_D$ | $H_E$ | L | $L_p$ | v | w | y | $Z_D^{(1)}$ | $Z_E^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 3.20 | 0.25<br>0.05 | 2.90<br>2.65 | 0.25 | 0.50<br>0.35 | 0.25<br>0.14 | 20.1<br>19.9 | 14.1<br>13.9 | 1 | 24.2<br>23.6 | 18.2<br>17.6 | 1.95 | 1.0<br>0.6 | 0.2 | 0.2 | 0.1 | 1.2<br>0.8 | 1.2<br>0.8 | $7^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT319-2 | | | | | | ~~95-02-04~~<br>97-08-01 |

## SOLDERING

### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

### Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

### Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

| CAUTION |
| --- |
| **Wave soldering is NOT applicable for all QFP packages with a pitch (e) equal or less than 0.5 mm.** |

**If wave soldering cannot be avoided, for QFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:**

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## DEFINITIONS

| **Data sheet status** | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |

## LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

**NOTES**

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